

In the claims:

Please amend the claims as indicated below.

1-18 (canceled)

19. (Currently Amended) A system comprising:

a Basic Input/Output System (BIOS);

a system bus coupled to said BIOS;

an integrated drive electronics (IDE) interface coupled to said system bus that receives disk drive requests from said BIOS via said system bus;

a striping controller coupled to said IDE interface;

a first disk drive including first IDE electronics, said striping controller coupled to said first IDE electronics;[and,]

a second disk drive including second IDE electronics, said striping controller coupled to said [striping controller] second IDE electronics, said first and said second IDE electronics each having data separator electronics, data formatting electronics and head positioning electronics; and

 said striping controller causes data being transmitted between said interface and said first and second drives to be written to and read from the first and second drives in an interleaved form and substantially in parallel.

20. (Previously Presented) The system of claim 19 wherein the data written to and read from the first and second disk drives is interleaved so that even sectors are accessed on the first disk drive and odd sectors are accessed on the second disk drive.

21. (Previously Presented) The system of claim 19 wherein the data being transmitted between the system bus and the first and second disk drives is subdivided into a plurality of sequential blocks.

22. (Previously Amended) The system of claim 21 wherein the first disk drive is accessed for every other block of data and the second disk drive is accessed for the remaining blocks.

23. (Previously Presented) The system of claim 19 wherein the BIOS transmits a system request that includes a sector bit string, a head bit string, a track bit string and a driver bit.

24. (Previously Presented) The system of claim 23 wherein the striping controller maps bits of the system request to a first system request data structure to be supplied to the first disk drive and a second system request data structure to be supplied to the second disk drive.

25. (Previously Amended) A method comprising:
transmitting an integrated drive electronics (IDE) request from a Basic Input/Output System (BIOS) onto a system bus;
receiving said IDE request at an IDE interface connected to said system bus;
transmitting said IDE request to a striping controller coupled to said IDE interface and first IDE electronics of a first disk drive and second IDE electronics of a second disk drive;

writing to and reading from the first disk drive and the second disk drive in an interleaved form and substantially in parallel in response to said IDE request.

26. (Previously Amended) The method of claim 25 further comprising receiving the IDE request at the striping controller.

27. (Previously Presented) The method of claim 25 wherein writing to and reading from a first disk drive and a second disk drive in an interleaved form comprises:
accessing even sectors on the first drive; and
accessing odd sectors on the second drive.

28. (Previously Amended) A striping disk controller comprising:
an integrated drive electronics (IDE) interface coupled to a system bus that receives disk drive requests from a Basic Input/ Output System (BIOS) separately coupled to said system bus; and
control logic coupled to the IDE interface and first disk electronics of a first disk drive and second disk electronics of a second disk drive, the control logic to cause data being transmitted via the system bus to be written to and read from a first disk drive and a second disk drive in an interleaved form and substantially in parallel.

29. (Previously Amended) The controller of claim 28 wherein the data written to and read from the first and second disk drives is interleaved so that even sectors are accessed on the first disk drive and odd sectors are accessed on the second disk drive.

30. (Previously Presented) The controller of claim 28 wherein the control logic subdivides the data being transmitted via the system bus into a plurality of sequential blocks.

31. (Previously Presented) The controller of claim 30 wherein control logic further accesses the first disk drive for every other block of data and accesses the second disk drive for the remaining blocks.

32. (Previously Presented) The controller of claim 28 wherein the control logic receives a system request that includes a sector bit string, a head bit string, a track bit string and a driver bit.

33. (Previously Presented) The controller of claim 32 wherein the control logic maps bits of the system request to a first system request data structure to be supplied to the first disk drive and a second system request data structure to be supplied to the second disk drive.

34. (Previously Presented) The controller of claim 28 wherein the control logic receives a system request intended for a single physical drive from the system bus.

35. (Previously Amended) A system comprising:
a central processing unit (CPU) that executes an operating system including a Basic Input/Output Operating System (BIOS);
a system bus coupled to the CPU;
an IDE interface coupled to the system bus that receives requests from the BIOS via the system bus;

a striping controller coupled to the IDE interface;

 a first storage device, including first IDE electronics, said striping controller coupled to said first IDE electronics; and

 a second storage device, including second IDE electronics, said striping controller coupled to said second IDE electronics;

 the striping controller, based on a standard IDE driver instruction, causes data being received to be written to and read from the first and second storage devices in an interleaved form and substantially in parallel.

36. (Previously Presented) The system of claim 35 wherein the data written to and read from the first and second drives is interleaved so that even sectors are accessed on the first storage device and odd sectors are accessed on the second storage device.

37. (Previously Presented) The system of claim 35, wherein the striping controller comprises:

 an exclusive-or (XOR) gate coupled to the IDE interface;

 a first FIFO memory coupled to the XOR gate and driven by a signal from the XOR gate to access the first storage device; and

 a second FIFO memory coupled to the XOR gate and driven by the signal from the XOR gate to access the second storage device.